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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit 2154
Examiner Larry D. Donaghue

In Re:	Mario D. Nemirovsky et al.
Case:	P3803
Serial No.:	09/312,302
Filed:	May 14, 1999
Subject:	**Interrupt and Exception Handling for Multi-Streaming Digital Processors**

To: The Commissioner of Patents and Trademarks
Washington, D.C. 20231

Dear Sir;

Response

All of the claims standing for examination are presented below for examination. Claims 1, 15 and 29 are amended in the present response.

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1. (Currently Amended) A multi-streaming processor system comprising:

a plurality of physical hardware streams for streaming one or more instruction threads;

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a set of functional resources for processing instructions from streams; and

interrupt logic;

wherein through the interrupt logic specific interrupts or exceptions are detected and at the time of their detection a specific stream of the plurality of physical hardware streams is directed to process the specific interrupt or exception.

2. (Original) The system of claim 1 wherein one interrupt or exception may be